Chip-Scale Energy and Power… and Heat

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Flexibility for Ultra Low Power

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Sub-threshold ($V_{DD}<V_T$) Survey

- Sub-threshold benefits
  – Leakage Power Decreases: 5X to 90X
  – Energy Consumption Decreases: 10X to 20X
  – E_{total}/operation minimized in sub-V_T
  – Aging Effects Improve: NBTI, EM, TDDB
- Challenges
  – Lower I_{on} / I_{off}
  – Variation
- State of art
  – Logic, SRAM, arithmetic units, processors, simple systems

Key Remaining Problems for Sub-threshold Operation in Systems

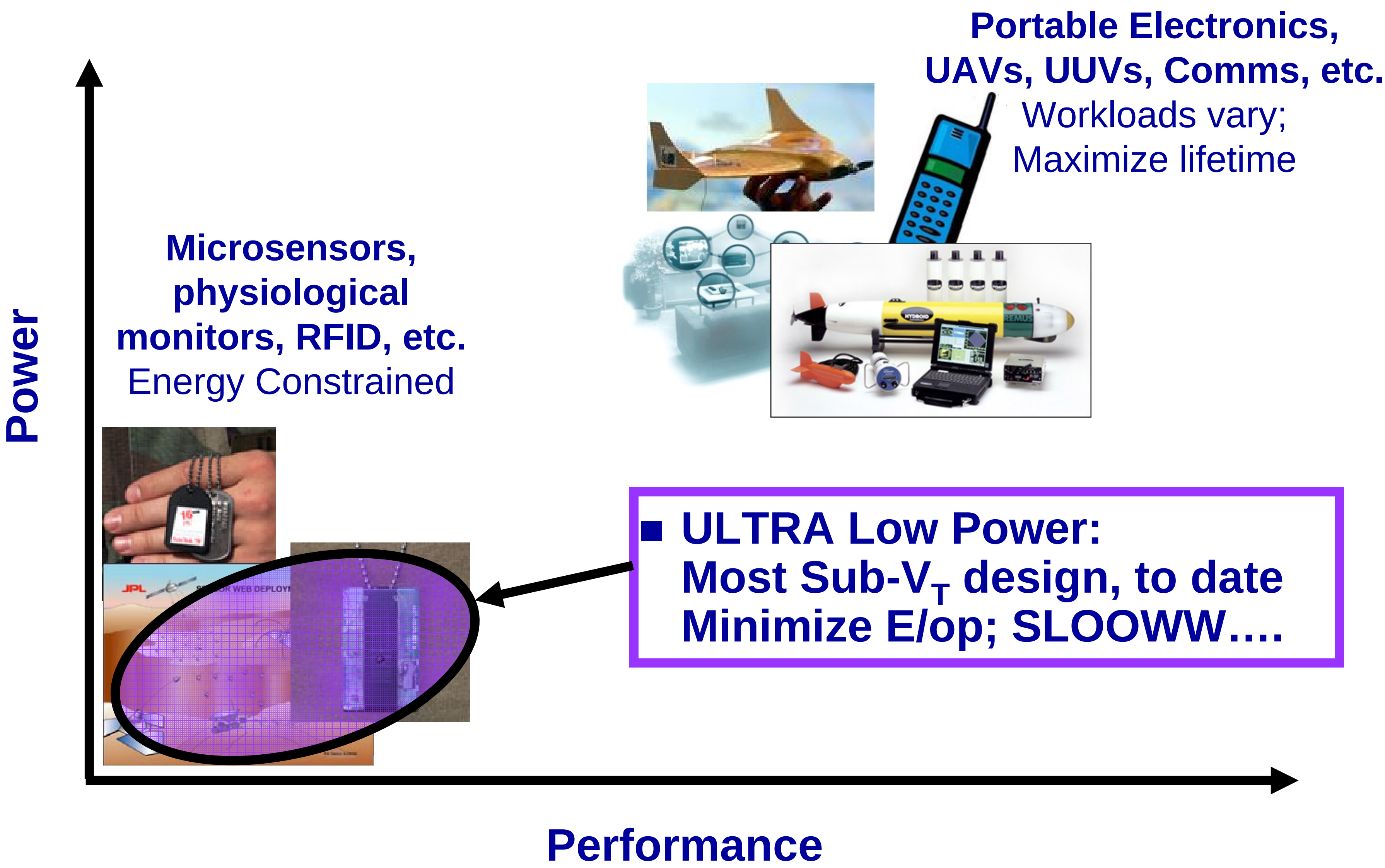
1. Very slow
2. Best efficiency comes from ASIC, but costly and slow for new applications
3. Digital power a small piece of pie in many ULP systems

Outline

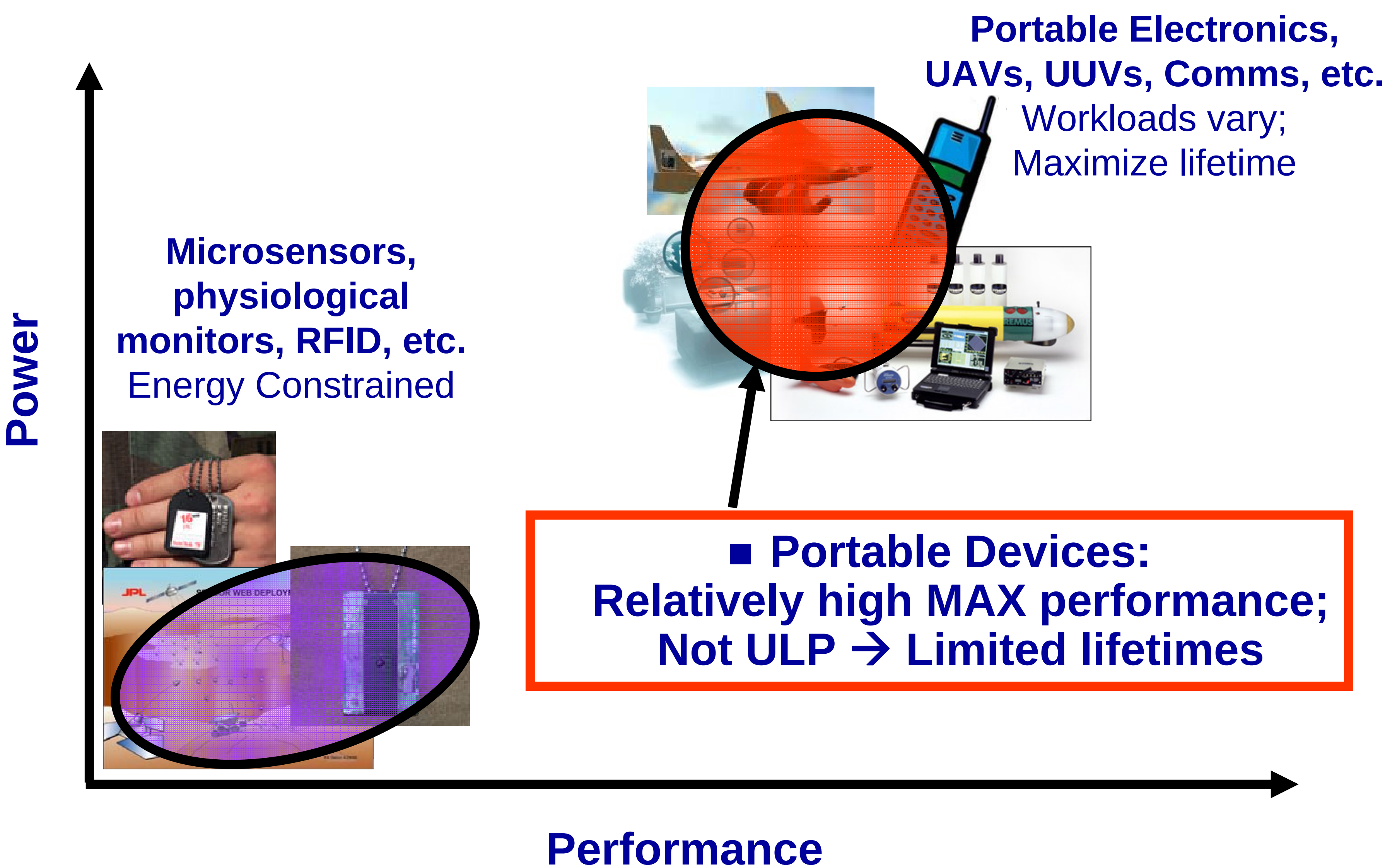
THESIS: Flexibility can help solve the key problems facing sub-threshold systems

- Energy / Performance Flexibility
- Hardware Flexibility
- System-Level Flexibility

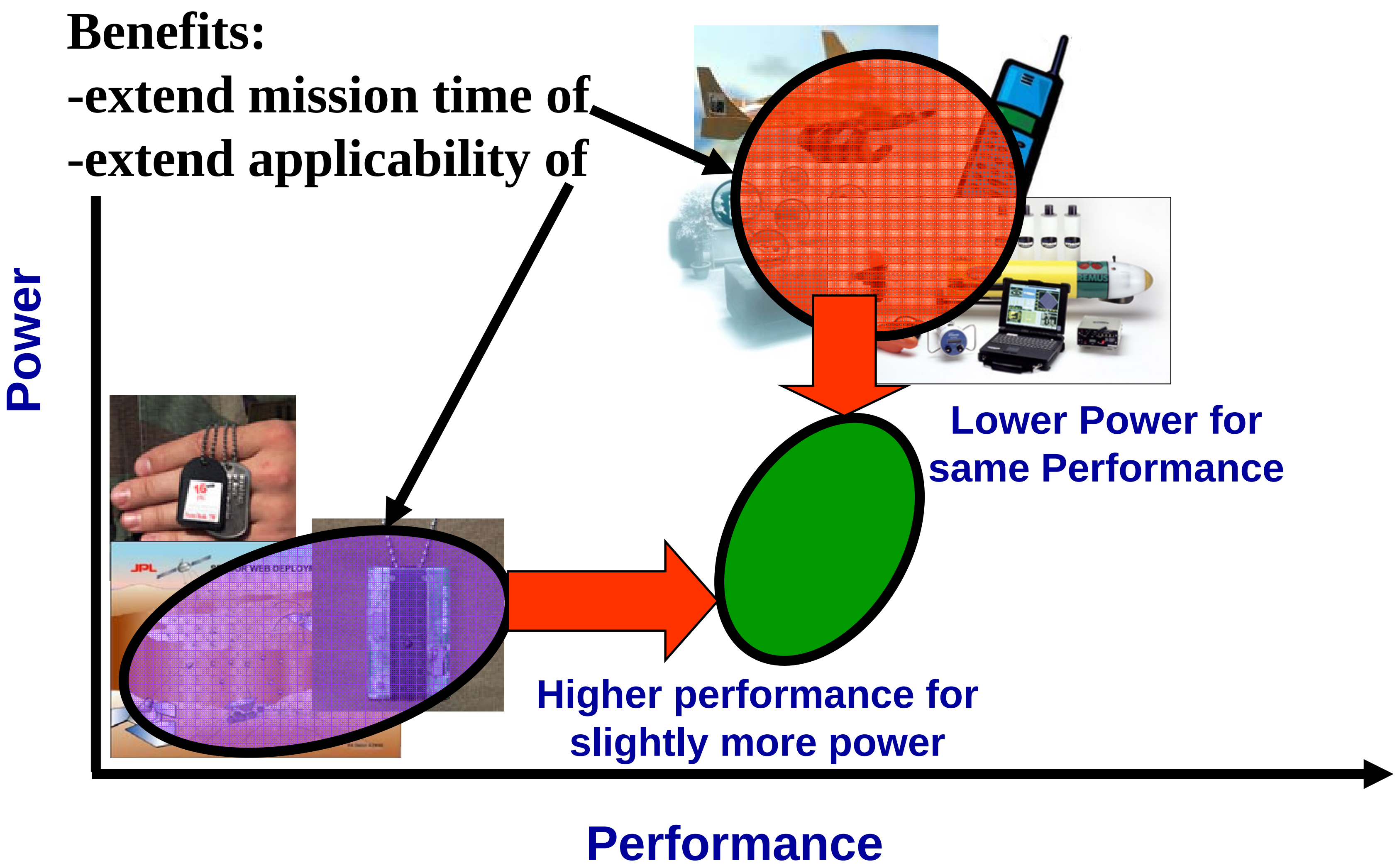
“Low Power” Application Space



"Low Power" Application Space



Proposed Energy/Performance Flexibility



How will we do this?

- Key insight: Definition of Performance

Old definition: Fixed speed or throughput

Accurate definition: Speed or throughput required to get "the job" done

"The job" changes:
→a range of performance requirements for a single app, depending on what is going on

Proposed Approach

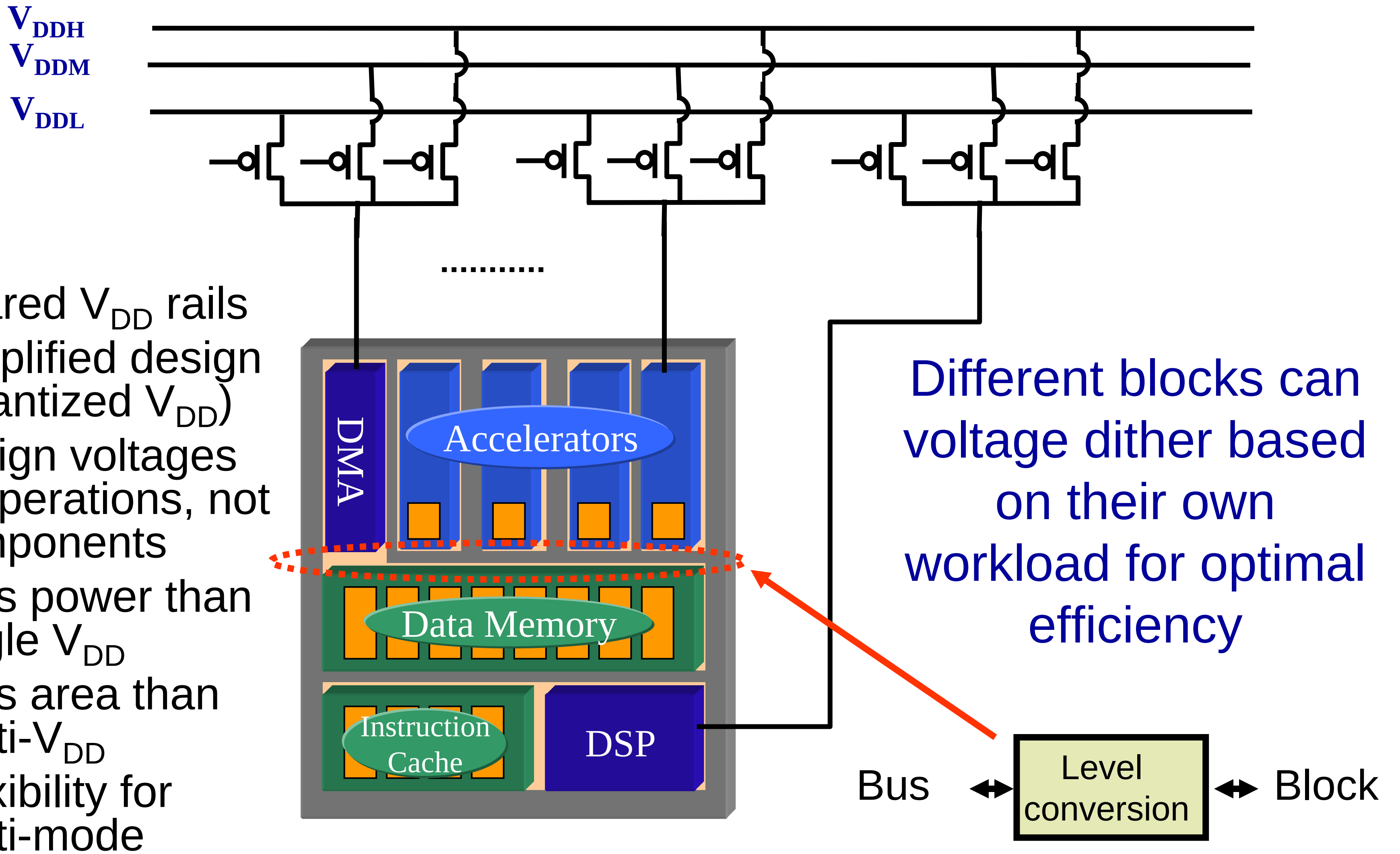
- Maximize efficiency of multi-V_{DD} design
  - Voltage is most effective knob

- Panoptic Dynamic Voltage Scaling (PDVS)
  - Multi-V_{DD}s (~2-4 voltage rails), local headers
  - Fully enables classical DVS
  - UDVS possible (hop to sub-threshold)
  - Finer *spatial* and *temporal* granularity
  - Multiple inherent power modes
  - Simple, low overhead implementation
  - LOTS of flexibility

[with J. Lach (UVA, ECE)]

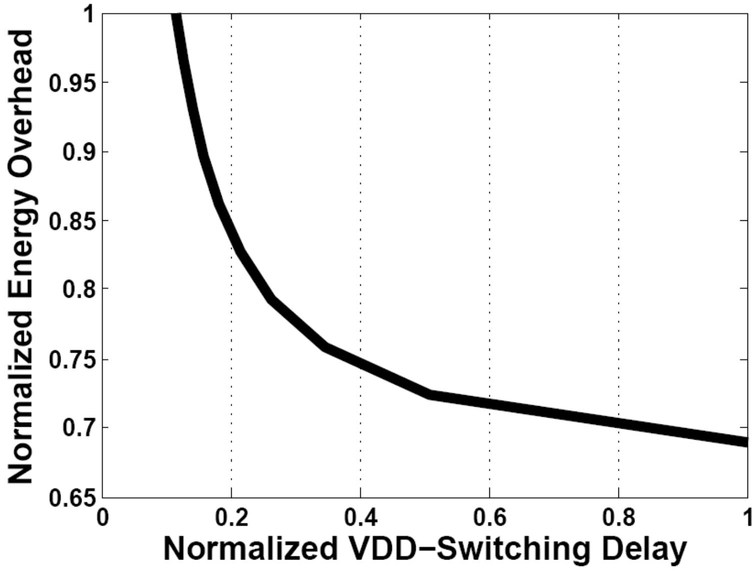
Example System: Apply PDVS to ASIC

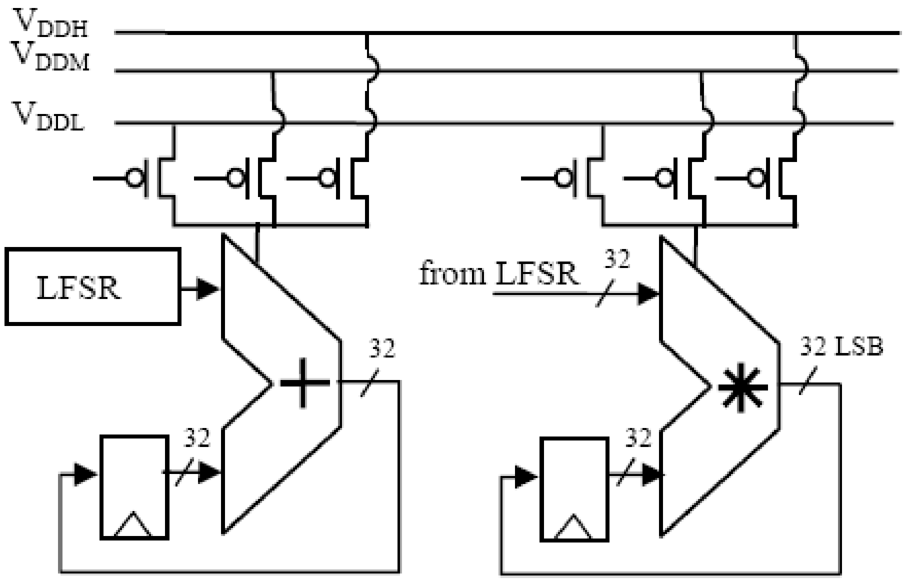
- Shared V_{DD} rails
- Simplified design (quantized V_{DD})
- Assign voltages to operations, not components
- Less power than single V_{DD}
- Less area than multi-V_{DD}
- Flexibility for multi-mode



Different blocks can voltage dither based on their own workload for optimal efficiency

V_{DD}-switching energy





90nm Test Chip

Measured E overhead to find number of cycles at V_L to break even: < 1!!

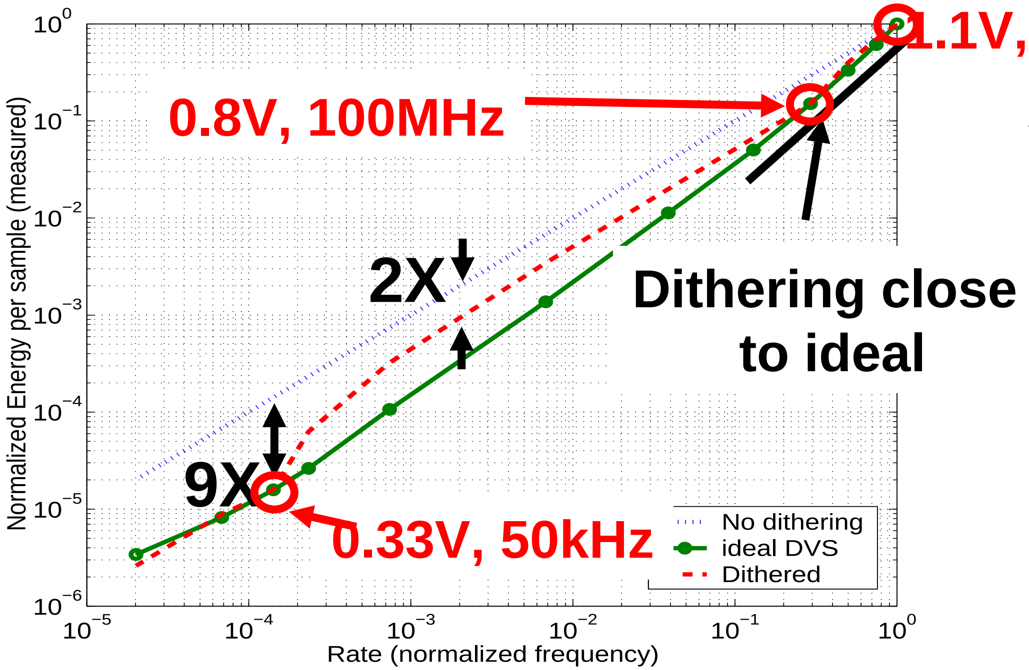
$$N_{BE} = \frac{(E_{High} - E_{Low})}{E_{switch}}$$

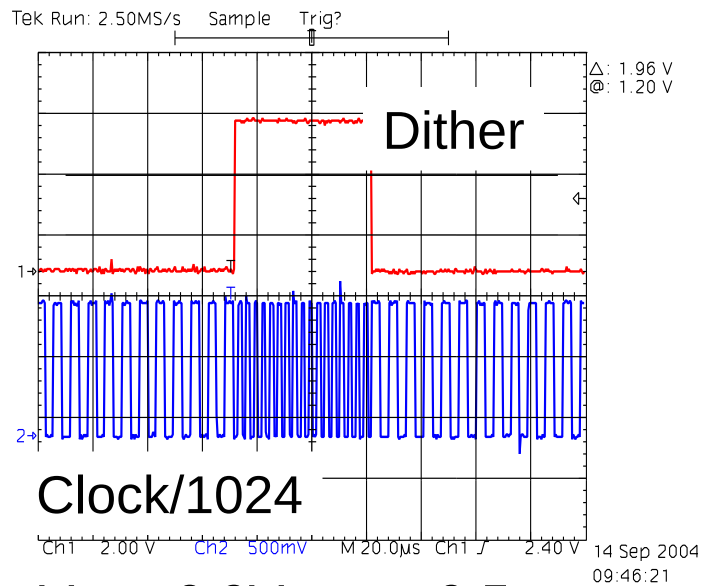
[ICCD, 2008]

Low Supply Voltage	Adder Break Even Cycles	Multiplier Break Even Cycles
0.9	0.689	0.436
0.8	0.579	0.408
0.7	0.607	0.263
0.6	0.721	0.328

UDVS: ULP (Sub-V_T) Option

Dither during high performance operation and switch to sub-threshold minimum energy operation when speed is not important





V_{DDL}=0.9V, rate=0.5

Calhoun & Chandrakasan, "Ultra-Dynamic Voltage Scaling Using Sub-threshold Operation and Local Voltage Dithering in 90nm CMOS," ISSCC, 2005.

Outline

- Energy / Performance Flexibility
- Hardware Flexibility
- System-Level Flexibility

The Problem: Many ULP Applications

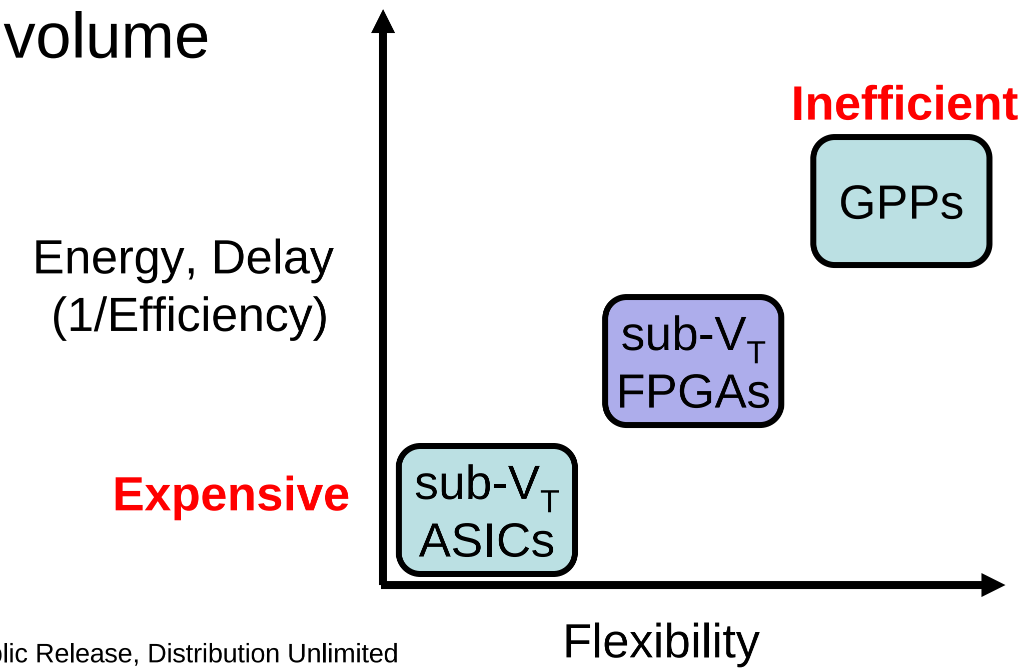
- Lots of apps (microsensors, RFID, tracking nodes, biotelemetry, micro-UAVs, hybrid insects, etc.)




- Need ULP (sub-V_T) for feasibility
- <u>Economics</u>: Often low volume

Sub-V_T FPGA:

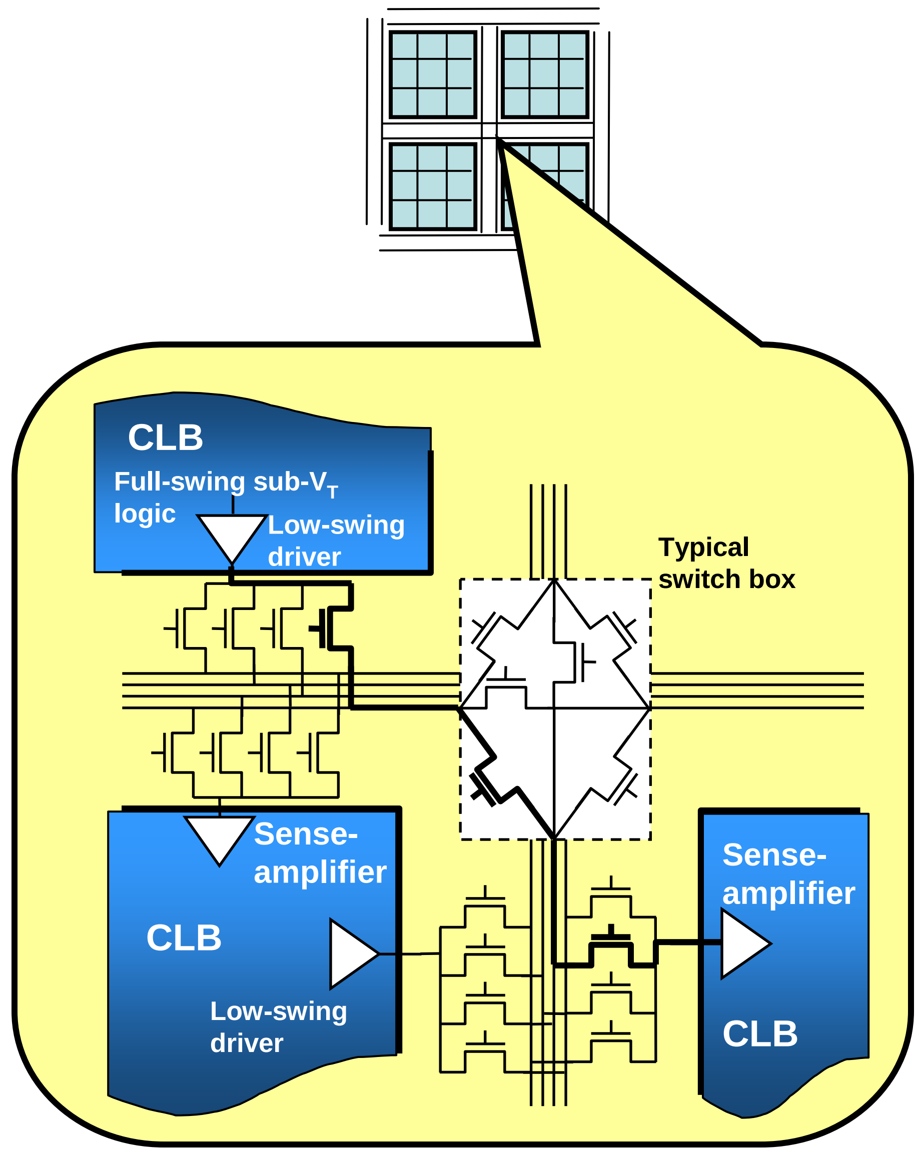
- Flexible, portable
- Low time-to-deployment
- Mission-specific efficiency
- Low unit cost



Ultra Low Power FPGA

- **Challenges to sub-V_T FPGA**
- **Variation, low I_{on}/I_{off}**
- **Interconnect dominates delay and power**

- **Approach**
  - **Low swing interconnect w/ sub-threshold sense amplifier**
  - **Regularity to reduce variation sources**
  - **Modified SRAM for config bits**
- **Anticipated Result**
  - **> 20X energy reduction**
  - **Tapeout spring 2009**



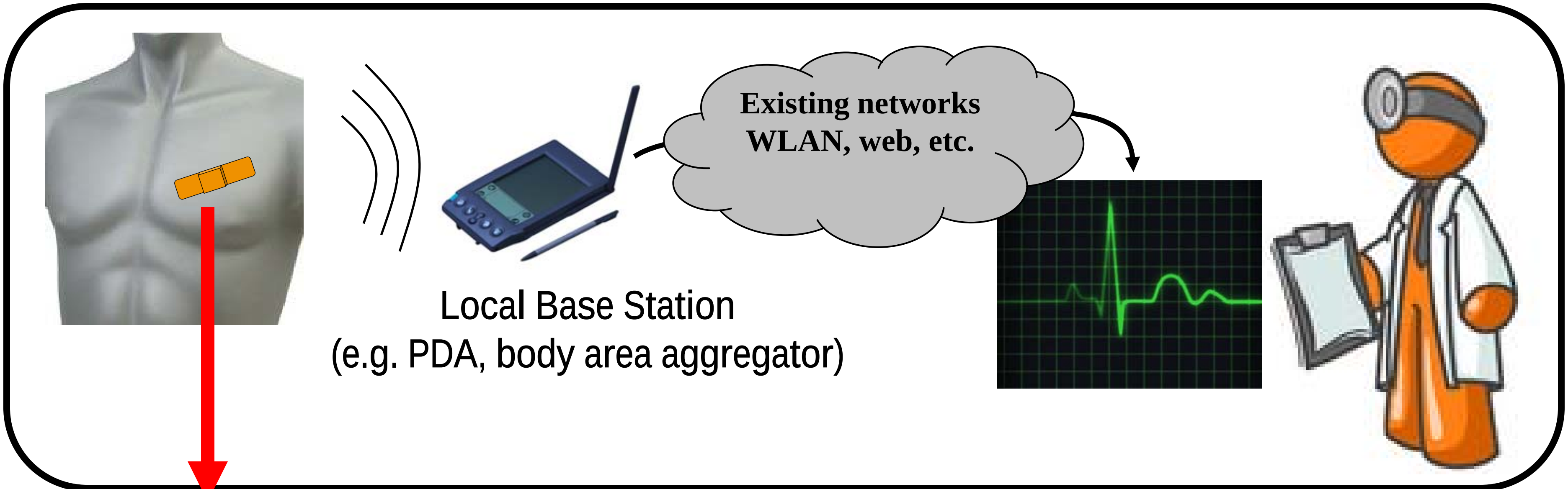
Outline

- Energy / Performance Flexibility
- Hardware Flexibility
- System-Level Flexibility

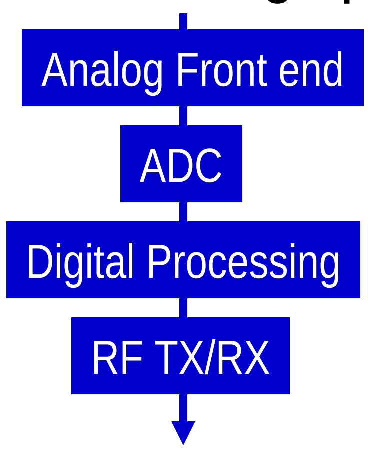
System Level Flexibility

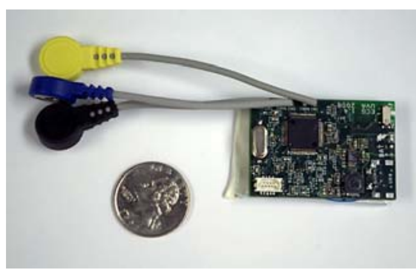
- Must consider system power breakdown
- Radio often dominates
- Leverage ULP digital (e.g. pre-process to reduce wireless data rate)
- Example system: ECG on a band-aid

Example: ECG Monitoring System

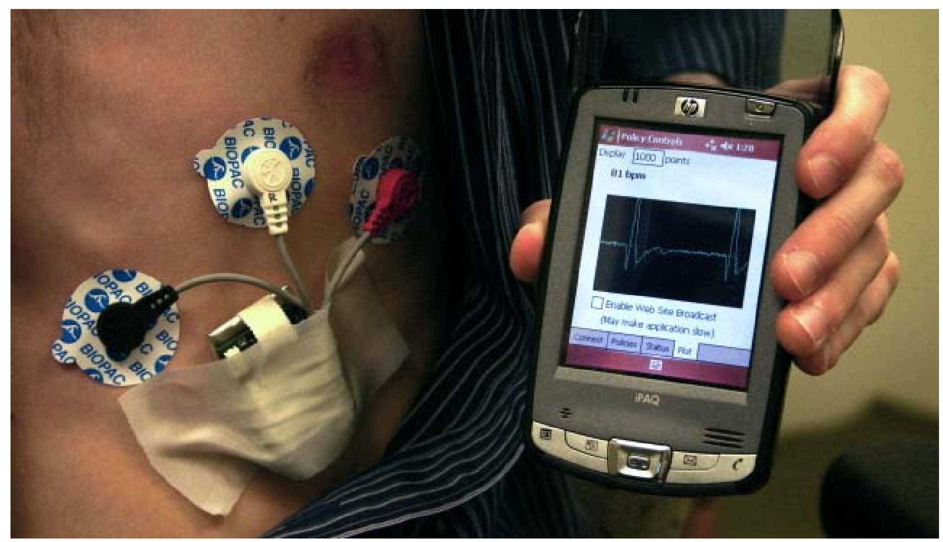


ECG sensing “patch”





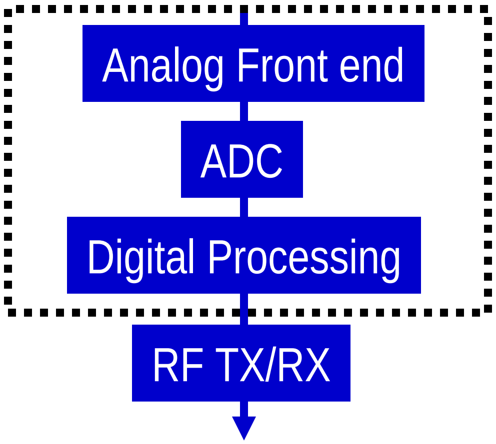
Discrete prototype

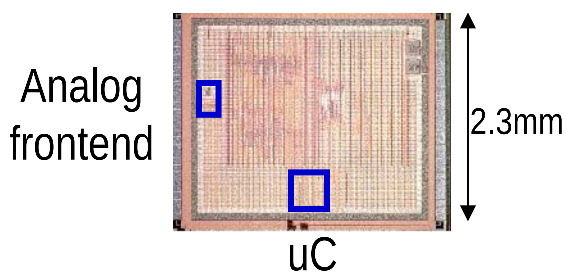


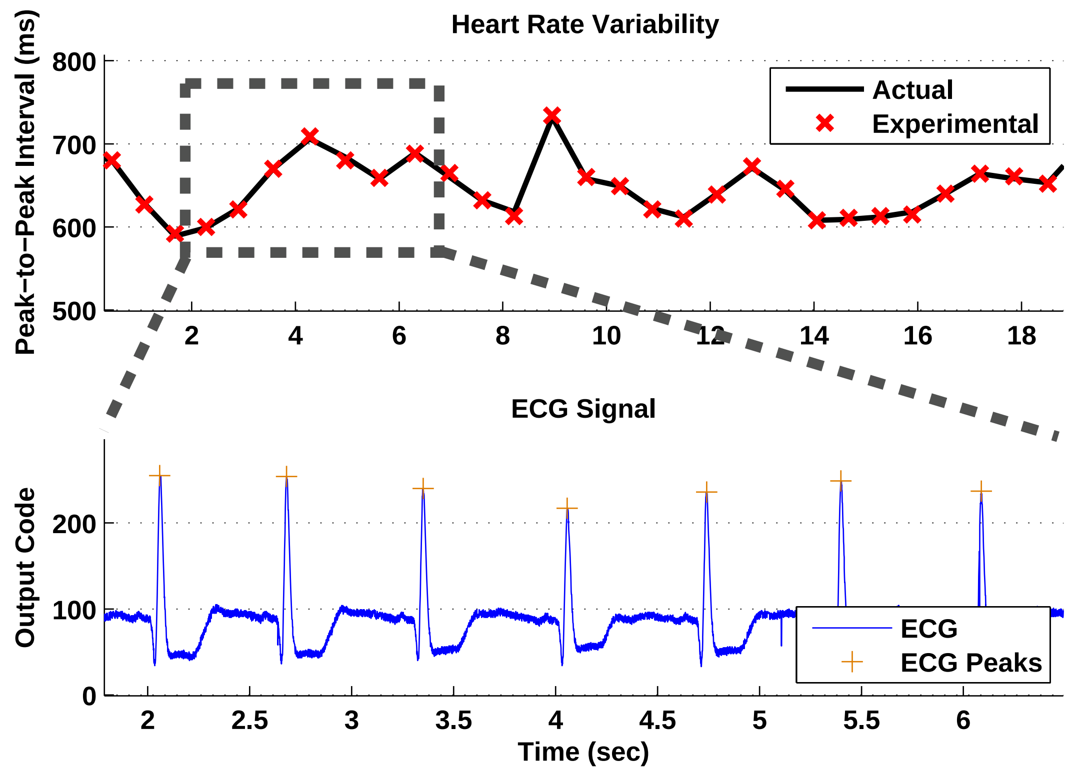
[with T. Blalock (UVA, ECE)]

Mixed Signal ECG System on Chip

ECG sensing “patch”







Leverage Sub-V_T processing by re-partitioning tasks at system level

Heart rate computation cuts wireless data rate by 500X

[with T. Blalock (UVA, ECE)]

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Conclusions

- Flexibility solves key problems for sub-V_T systems
  - Energy/performance flexibility
  - Hardware flexibility
  - System flexibility

- Thank you! Any questions?


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